**Tugas Rangkaian Logika 2   
‘Binary to Gray using VHDL’**

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**1. Tabel Kebenaran**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Input : Biner | | | | Output : Grey | | | |
| A | B | C | D | G1 | G2 | G3 | G4 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

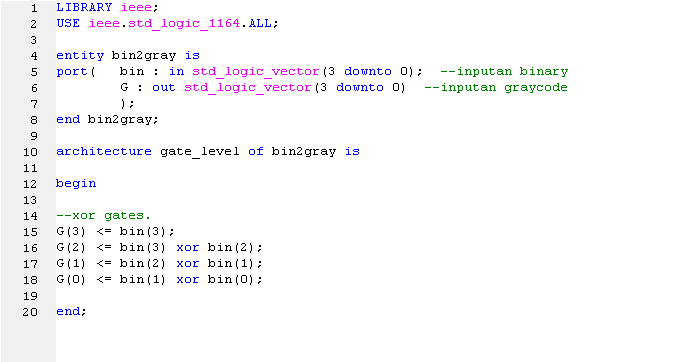
**2. K-Map dan Persamaan Boolean**

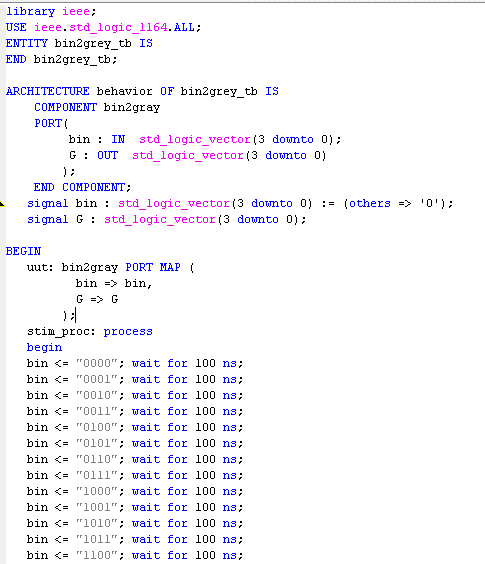
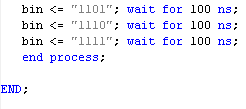
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| G1 | : A |  |  |  |
|  |  |  |  |  |
|  | 00 | 01 | 11 | 10 |
| 00 |  |  |  |  |
| 01 |  |  |  |  |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 1 | 1 | 1 | 1 |

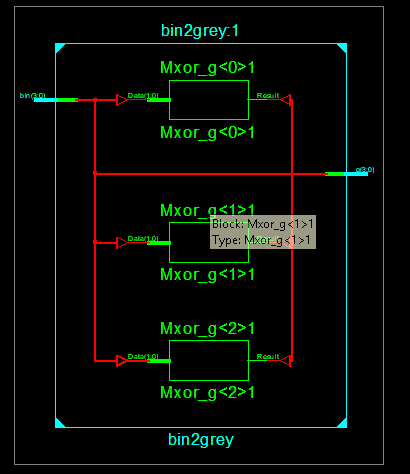
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| G2 | : BC’ + B’C | | : B xor C |  |
|  |  |  |  |  |
|  | 00 | 01 | 11 | 10 |
| 00 |  |  | 1 | 1 |
| 01 | 1 | 1 |  |  |
| 11 | 1 | 1 |  |  |
| 10 |  |  | 1 | 1 |

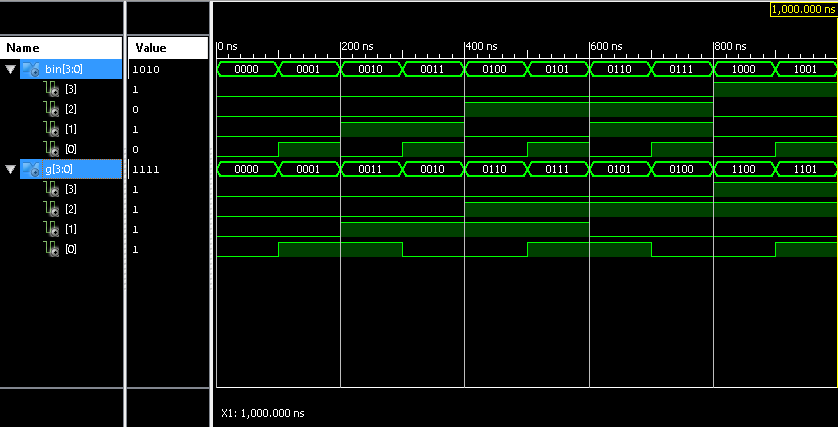
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| G3 | : A’B + B’A | | : A xor B |  |
|  |  |  |  |  |
|  | 00 | 01 | 11 | 10 |
| 00 |  |  |  |  |
| 01 | 1 | 1 | 1 | 1 |
| 11 |  |  |  |  |
| 10 | 1 | 1 | 1 | 1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| G4 | : C’D + CD’ | | : C xor D |  |
|  |  |  |  |  |
|  | 00 | 01 | 11 | 10 |
| 00 |  | 1 |  | 1 |
| 01 |  | 1 |  | 1 |
| 11 |  | 1 |  | 1 |
| 10 |  | 1 |  | 1 |

**3. Program VHDL**   


**4. Testbench  
  
**

**5. RTL Schematic**

**6. Timing diagram :**

**7. Analisa**Kode ini disimulasikan menggunakan Xilinx ISE 14.5 Tool. Adapun Rangkain Digital untuk mengkonversikan Biner Code ke Gray Code, ataupun sebaliknya, dapat menggunakan 3 buah komponen Gerbang Exclusive OR 2 Input atau Dual XOR Gates dengan susunan input dan output. Timing diagram juga memastikan kebenaran design program biner ke graycode yang telah dibuat.

**‘Binary to 2421 using VHDL’**

**1. Turth Table**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| binary | | | | 2421 | | | |
| A0 | A1 | A2 | A3 | W0 | W1 | W2 | W3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | D | D | D | D |
| 1 | 0 | 1 | 1 | D | D | D | D |
| 1 | 1 | 0 | 0 | D | D | D | D |
| 1 | 1 | 0 | 1 | D | D | D | D |
| 1 | 1 | 1 | 0 | D | D | D | D |
| 1 | 1 | 1 | 1 | D | D | D | D |

**2. K-Map**

W0 :

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| D | D | D | D |
| 1 | 1 | D | D |

W1 :

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| D | D | D | D |
| 1 | 1 | D | D |

W2:

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| D | D | D | D |
| 1 | 1 | D | D |

W3:

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| D | D | D | D |
| 0 | 1 | D | D |

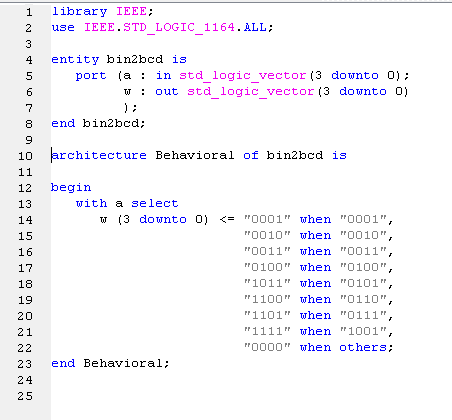
**3. Boolean Equation**

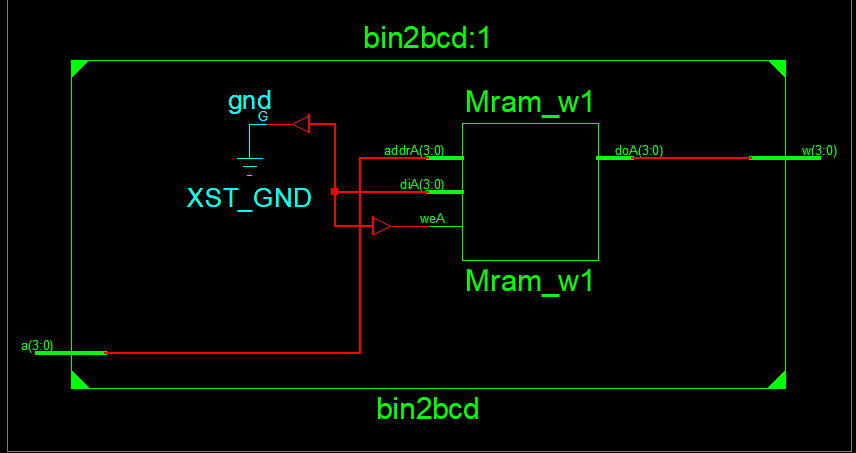
W0 = A + CD + BC

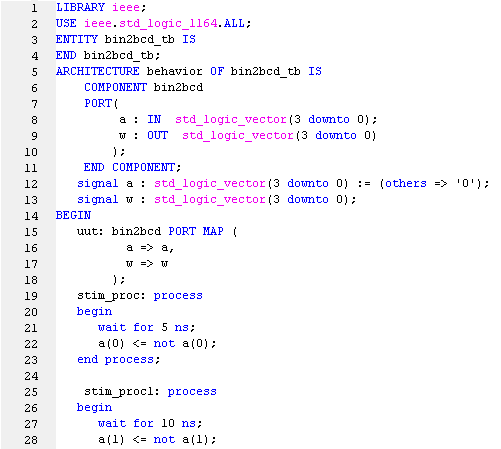
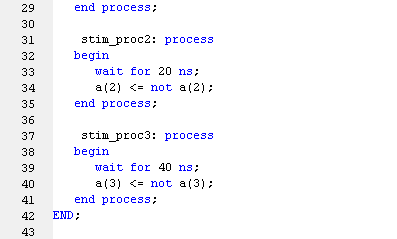
W1 = A + BD’ + BC

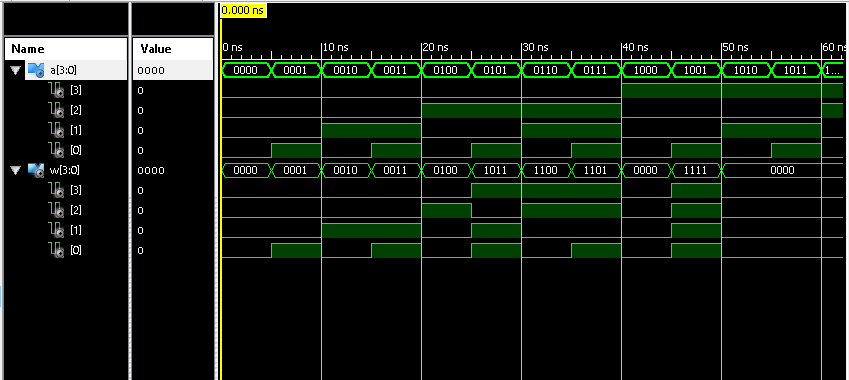
W2 = A + BC’D + B’C

W3 = D

**4. Program VHDL**  


**5. RTL Schematic**  


**6. Test Bench**   
  


**7. Timing Diagram**  
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**8. Analisa**   
praktikum kali ini, kita membuat sebuah program menggunakan bahasa VHDL yang berfungsi untuk mengonversikan biner ke kode 2421, sebelum itu kita harus membuat tabel kebenaran terlebih dahulu yang nantinya dapat digunakan untuk membuat program VHDL, selanjutnya buat K-mapnya, sebenarnya K-Map disini bertujuan untuk mendapatkan persamaan boolean dengan mudah yang mana nanti persamaan tersebut dapat digunakan sebagai persamaan variable yang ada pada program VHDL nantinya, std\_logic\_vector sendiri digunakan untuk pembuatan array yang nantinya setiap index mempresentasikan sebuah bit biner maupun kode 2421, bit yang digunakan pada praktikum ini adalah 4, karenanya kita tuliskan (3 down to 0), jika ketika menjalankan simulasi testbench dan mendapatkan value uuuu (undifined) langkah yang harus dilakukan adalah menginisialisasi *value* (nilai) pada bit.